

WHAT IS CLAIMED IS:

- 1 1. A hardware-reconfigurable digital filter having multiple filtering modes,
2 comprising:
3 logic circuitry adapted to process data corresponding to input data, the logic
4 circuitry including an X-by-Y array of registers for supporting at least one first filtering
5 mode using the registers arranged linearly and for supporting at least one second
6 filtering mode using the registers arranged nonlinearly, wherein each of X and Y is at
7 least 2;
8 computational circuitry adapted to perform computations responsive to the logic
9 circuitry and including at least Y multiplication logic circuits and at least Y addition
10 logic circuits; and
11 mode selection circuitry adapted to switch the digital filter between the multiple
12 filtering modes.
- 1 2. The hardware-reconfigurable digital filter of claim 1, wherein the logic circuitry
2 and the computational circuit are configurable, in response to the mode selection
3 circuitry, to operate in at least two of the following filtering modes: polyphase direct,
4 polyphase transposed, finite-impulse response 11-tap, and finite-impulse response 12-
5 tap.
- 1 3. The hardware-reconfigurable digital filter of claim 1, wherein each of the
2 multiplication and addition logic circuits along a Y-axis direction has reconfiguration
3 circuitry adapted to reconfigure the multiplication and addition logic circuits along the
4 Y-axis direction the logic circuitry in response to the mode selection circuitry,
5 and the first filtering mode supports an impulse response filtering mode and the second
6 filtering mode supports at one polyphase filtering mode and another impulse response
7 filtering mode.

1 5. The hardware-reconfigurable digital filter of claim 4, wherein the mode selection
2 circuitry adapted to switch the digital filter between the polyphase transposed filtering
3 mode and another one of the modes.

1 7. The hardware-reconfigurable digital filter of claim 6, wherein the first selection
2 circuit is adapted to reconfigure the computational circuitry, and the second selection
3 circuit is adapted to reconfigure the logic circuitry.

1 9. The hardware-reconfigurable digital filter of claim 1, wherein the logic circuitry
2 and the computational circuit are configurable to support saving and loading video data
3 for context switching and switching back and forth among multiple long input lines.

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1 11. The hardware-reconfigurable digital filter of claim 1, wherein each of a first
2 plurality of the registers in the array is adapted as a first sliced circuit along an axis
3 defined by an alignment of the Y registers, and each of a second plurality of the
4 registers in the array is adapted as a second sliced circuit along an axis defined by an
5 alignment of the Y registers.

1 12. A hardware-reconfigurable digital filter having multiple filtering modes,
2 comprising:

3 logic circuitry adapted to process and mirror data corresponding to filter inputs
4 about a data point corresponding to selected target node in a video image segment, the
5 logic circuitry including an X-by-Y array of registers, wherein Y is greater than X and
6 X is at least 2;

7 a computational circuit adapted to perform computations responsive to the logic
8 circuitry and including at least Y multiplication logic circuits and at least Y addition
9 logic circuit; and

10 mode selection circuitry adapted to direct the digital filter into a polyphase
11 transposed filtering mode by configuring the logic circuitry and the computational
12 circuitry for processing data using the registers in a linear array and to direct the digital
13 filter into another filtering mode by configuring the logic circuitry and the
14 computational circuitry for processing data using the registers in a nonlinear array.

1 13. The hardware-reconfigurable digital filter of claim 12, wherein a plurality of the
2 registers in the array is adapted as sliced circuits.

1 14. The hardware-reconfigurable digital filter of claim 12, wherein a plurality of the
2 registers in the array is adapted as sliced circuits along an axis defined by an alignment
3 of the Y registers.

1 15. The hardware-reconfigurable digital filter of claim 12, wherein each of a first
2 plurality of the registers in the array is adapted as a first sliced circuit along an axis

3 defined by an alignment of the Y registers, and each of a second plurality of the
4 registers in the array is adapted as a second sliced circuit along an axis defined by an
5 alignment of the Y registers.

1 16. The hardware-reconfigurable digital filter of claim 12, wherein X is equal to two
2 and Y is not less than 6, and wherein the multiple filtering modes include the polyphase
3 transposed filtering mode, a polyphase direct filtering mode, and two FIR filtering
4 modes, one of the FIR filtering modes including more taps than the other of the two FIR
5 filtering modes.

1 17. The hardware-reconfigurable digital filter of claim 16, wherein one of the FIR
2 filtering modes includes 12 taps.

1 18. A hardware-reconfigurable digital filter having multiple filtering modes,
2 comprising:

3 logic means for processing data corresponding to input data, the logic means
4 including an X-by-Y array of registers for supporting at least one first filtering mode
5 using the registers arranged linearly and for supporting at least one second filtering
6 mode using the registers arranged nonlinearly, wherein each of X and Y is at least 2;

7 selection means adapted to switch the digital filter between different ones of the
8 multiple filtering modes; and

9 computational means adapted to perform computations responsive to the logic
10 means and including at least Y multiplication logic circuits and at least Y addition logic
11 circuits.

1 19. A hardware-reconfigurable digital filter having multiple filtering modes,
2 comprising:

3 logic means for processing and mirroring data corresponding to filter inputs
4 about a data point corresponding to selected target node in a video image segment, the
5 logic circuitry including an X-by-Y array of registers for supporting at least one first

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6 filtering mode using the registers arranged linearly and for supporting at least one
7 second filtering mode using the registers arranged nonlinearly, wherein Y is greater than
8 X and X is at least 2;

9 means for switching the digital filter between a polyphase transposed filtering
10 mode and at least one other mode of the multiple filtering modes; and

11 means for performing computations responsive to the logic means and including
12 at least Y multiplication logic circuits and at least Y addition logic circuits, each of the
13 multiplication and addition logic circuits having reconfiguration means responsive to
14 the switching means.

1 20. The hardware-reconfigurable digital filter of claim 19, wherein sets of the Y
2 multiplication logic circuits and Y addition logic circuits are sliced circuits.

1 21. A hardware-reconfigurable digital filter having multiple filtering modes,
2 comprising:

3 logic circuitry adapted to process data corresponding to input data, the logic
4 circuitry including a 2-by-6 array of registers for supporting a 12-tap FIR filtering mode
5 using the registers arranged linearly and, using the registers arranged nonlinearly, for
6 supporting an 11-tap FIR filtering mode in which two of the registers at an end of the
7 array are paired, a polyphase direct filtering mode in which each of six pairs of the
8 registers is used to combine a single input to the pair, and polyphase transposed filtering
9 mode in which six pairs of the registers are used to provide a wide bitwidth
10 corresponding to a high-precision number;

11 computational circuitry adapted to perform computations responsive to the logic
12 circuitry and including a multiplication logic circuit and an addition logic circuit,
13 separately arranged, for receiving and processing data from each of the six pairs of
14 registers; and

15 mode selection circuitry adapted to switch the digital filter between the multiple
16 filtering modes.